SPECIFICATION

Title of the Invention

A MATRIX DISPLAY APPARATUS AND A DRIVING METHOD THEREOF

Background of the Invention

(1) Field of the Invention:

The present invention relates to a matrix display apparatus and its driving method, particularly to the display apparatus and the driving method capable of uniform brightness display, furthermore lowering signal voltages and power consumption.

(2) Description of the Prior Art

One of the important subjects of a liquid crystal display apparatus is lowering the driving voltage. Lowering the driving voltage brings about improvement of such as picture quality deterioration as non-uniform brightness in a display panel and power consumption reduction. Furthermore, the reliability of circuits in the display apparatus can be improved and the lower price of it can be realized by downsizing driving circuits. Especially in using MOS-LSI to a driving circuit, the price of the display apparatus is more lowered because the area of a LSI chip can be made into small size. As mentioned above, it is very profitable to the picture quality, the power consumption and the price to lower the driving voltage of a liquid crystal display.

Various method for lowering the driving voltages are

presented. One of them is described in "SOCIETY FOR INFORMATION DISPLAY INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS,(1989),pp242-244". The method described in the paper changes the scanning voltage and the counter electrode voltage in pulse wise, in-phase and by the same amplitude, adjusting to the scanning timing for lowering the signal voltage(source voltage) of the voltages driving TFT(Thin Film Transistor) liquid crystal matrix panel. By the method, the amplitudes of signal voltages can be lowered ,but the waveform distortion of counter electrode voltages and a scanning voltage increases since parasitic capacitances and resistances of wiring increase due to increase of the size of the liquid crystal panel. Therefore, the voltage applied to the liquid crystal changes depending to the pattern displayed on the panel, and the non-uniform brightness and the deterioration of picture quality occurs in the panel thereby. Especially, in a high resolution liquid crystal panel having about a thousand of scanning lines,the influences of the waveform distortion becomes severe and the picture quality deterioration occurs significantly due to short scanning time of one line. Another method for lowering the signal voltage is also described "SOCIETY FOR INFORMATION DISPLAY INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS,(1992), pp47-50". Although it is possible to reduce the deterioration of the picture quality due to the waveform distortion of the scanning voltages and the counter electrode voltages and to lower the driving voltage, direct

current voltages are superposed on the voltages applied to the liquid crystal unless the parasitic capacitances between TFT terminals and the storage capacitances are uniform over the panel. Thereby, the phenomena of elongation of a display renewing time , namely, afterimage occurs. The reliability of the liquid crystal decreases by the superposition of the direct current voltage on the liquid crystal. The storage capacitances and the parasitic capacitances have considerable non-uniformity in the panel when the panel size is as 10-15 inches large as the display panel size of personal computers. The non-uniformity is induced by the cause that the accuracy of photo-mask adjustment and etching in the process of TFT producing degrades in proportion as the panel size becomes large. So the reliability deterioration of the liquid crystal and the afterimage occurrence become more significant as the panel size increases. Other methods for decreasing the signal voltage are presented Japan Laid Open 913/1990 and Japan Laid Open 145490/1992. The methods do not resolve the problem of poor picture quality such as the striped picture in the horizontal direction (referred to the smearing).

Summary of the Invention

(1) Object of the Invention

Objectives of the present invention are providing a display apparatus and a drive method thereof for lowering the signal voltages of the liquid crystal matrix panel without deteriorating the picture quality, for reducing

non-uniformity of brightness over the panel caused by non-uniformity of output voltages of the drive circuit and the parasitic capacitances between terminals of TFTs and for preventing the smearing in a displayed picture.

(2) Method Solving the Problems

In order to attain the above mentioned objectives, the present invention presents a matrix panel display apparatus having plural signal lines and plural scanning lines intersecting each other and, near each intersection point, a picture element including a picture element electrode, a counter electrode, a display medium between the two electrodes and a transistor for applying image signals from the signal line to the picture element electrode controlled based on the scanning signals from the scanning line, which said apparatus comprises;

means for generating auxiliary signals for increasing the effective voltages of the image signals and applying the auxiliary signals to the picture elements while each of the transistor is non-conducting and each of the picture element is not selected, and thereof .

The present invention also presents a matrix panel display apparatus having plural signal lines and plural scanning lines intersecting each other and, near each intersection point, a picture element including a picture element electrode, a counter electrode, a display medium between said two electrodes and a transistor for applying image signals from said signal line to said picture element electrode controlled based on said scanning signals from

said scanning line, which said apparatus comprises;

picture signal generating means in a signal circuit for dividing the plural picture elements selected at the same time into two groups and for applying first picture signal group to the first group of picture elements and second picture signal group having the polarity reverse to the former signal group to said second group of picture elements, and

bias signal generating means for applying first bias signals having the polarity reverse to the first picture signal group to the first group of picture elements through storage capacitances in the first group of picture elements , and second bias signals having the polarity reverse to the second picture signal group to the second group of picture elements through storage capacitances in the second group of picture elements during selection period of the first and second group of picture elements, and a driving method thereof.

And liquid crystal is used as the display medium in the optimal embodiment.

Brief Description of the Drawings

Fig.1 shows a conceptual diagram of the whole matrix display apparatus by the present invention.

Figs.2(a) and 2(b) show example equivalent circuits of the picture elements in the matrix display apparatus.

Fig.3 shows example operations of the picture element in the matrix display apparatus.

Fig.4 shows the first embodiment of the liquid crystal matrix display panel.

Fig.5 shows the second embodiment of the liquid crystal matrix display panel.

Fig.6 shows an example driving timing of the liquid crystal matrix display panel.

Fig.7 shows an example fundamental waveform of the voltage applied to the picture element in the present invention.

Fig.8 shows an example driving timing in the present invention.

Fig.9 shows an example relation between the effective voltage applied to liquid crystal to the amplitude of a signal voltage (comparing two cases with and without the auxiliary signal).

Fig.10 shows an example relation between the brightness of liquid crystal to the amplitude of a signal voltage (comparing two cases with and without the auxiliary signal).

Fig.11 shows the equivalent circuit and the driving timing in the third embodiment.

Fig.12 shows the equivalent circuit of the display picture element part in the fourth embodiment.

Fig.13 shows an example of auxiliary signal generation means in the fifth embodiment.

Fig.14 shows the circuit constitution of the sixth embodiment.

Fig.15 shows the plane structure of the picture

element in the sixth embodiment.

Fig.16 shows the driving voltage waveforms in the sixth embodiment.

Fig.17 shows a block diagram of the signal voltage generation part in the seventh embodiment.

Fig.18 shows the constitution of the signal driving LSI in the eighth embodiment.

Fig.19 shows the driving voltage wavesforms in the ninth embodiment.

Fig.20 shows the driving voltage wavesforms in the tenth embodiment.

Fig.21 shows the plane structure of the picture element in the eleventh embodiment.

Fig.22 shows the circuit constitution in the twelfth embodiment.

Fig.23 shows the driving voltage waveforms in the twelfth embodiment.

Fig.24 shows the circuit constitution in the thirteenth embodiment.

Fig.25 shows the driving voltage waveforms in the thirteenth embodiment.

Fig.26 shows the plane constitution of the storage capacitance in the fourteenth embodiment.

Fig.27 shows the strength of transmitted light to the voltage applied to liquid crystal.

Fig.28 shows the equivalent circuit of the two adjoining picture elements.

Detailed Description of the Embodiments

Hereinafter, details of the present invention is explained based on embodiments referring to drawings.

(Embodiment 1)

A conceptual figure of a whole constitution of the display apparatus by the present invention is shown in Fig.1. The display apparatus comprises a matrix panel 1 consisting of scanning lines 2, signal lines 3, picture elements 4 provided at the intersection points of where the lines 2 and the lines 3 cross each other, a scanning circuit 5 and a signal circuit 6 generating the predetermined voltages and applying them the scanning lines 2 and the signal lines 3, respectively, a display control circuit 8 generating timing signals to the scanning circuit 5, the signal circuit 6 and a auxiliary signal for increasing the effective value of the signal voltages generating circuit 10, a system circuit 9 connected to the display control circuit 8, the auxiliary signal generating circuit 10 and a auxiliary signal information generating circuit 11 connected to the auxiliary signal generating circuit 10 through a auxiliary signal line 13. As to the picture elements 4, any combination of switching elements and such display material as liquid crystal, electroluminescence and so on is applicable and not restricted to any specific material combinations. And the brightness or the gradation number of the picture elements is not restricted to any specific value. The auxiliary signal Vsub is inputted into a display part 7 consisting of

the scanning circuit 5, the signal circuit 6 and the matrix panel 1 through a auxiliary signal inputting line 12. Examples of Vsub are described later. As shown in Fig.1, the present invention is characterized by the process of selecting each picture element in turn by the scanning circuit 5, applying the picture signal voltage to the selected picture element by the signal circuit(a first driving means), applying the auxiliary signal Vsub obtained by the auxiliary signal generating circuit(a second driving means) to each picture element in the display part and displaying any pictures on the matrix panel by driving the matrix panel with the synthesized signals of generated signals by the first and second driving means. The auxiliary signal information generating means 11 generates the information for deciding waveform of the auxiliary signal based on the environmental conditions such as temperature, the display picture quality conditions such as the brightness or the contrast of the picture elements and so forth, and inputs the information into the auxiliary signal generating circuit 10. The information from the system circuit 9 may be directly inputted into the auxiliary signal generating circuit 10.

An embodiment of the present invention is explained by taking a liquid crystal display apparatus as an example in the followings. Equivalent circuit examples of the picture elements 4 in the liquid crystal display apparatus are shown in Figs.2(a) and 2(b). The liquid crystal 17 is driven by such a switching element 16 as a TFT. A MOS

transistor or a bipolar transistor besides a TFT is also applicable to the switching element. The storage capacitances 18 connected in parallel with the liquid crystal 17 is necessarily not needed,but providing such storage capacitances is convenient to constituting a flexible display apparatus. The difference between the equivalent circuit of Fig.2(a) and that of Fig.2(b) is in that a terminal of the storage capacitance 18 is connected to a storage capacitance voltage inputting terminal 20 or to the scanning line 15. Fig.4 shows an embodiment of the present invention of which the equivalent circuit of the picture elements 4 is described as that of Fig.2(a). One picture element is consisted of the TFT 16, the liquid crystal 17 and the storage capacitance 18, and the total picture elements are arranged in the distributed dots state of (m × n) matrix . A terminal of each liquid crystal 17 is connected to a TFT 16 and the other terminal of the liquid crystal 17 is connected to the auxiliary signal generating circuit 10. A terminal of each storage capacitance 18 is connected to a TFT 16 and the other terminal of the storage capacitance 18 is connected to the storage capacitance voltage inputting terminal 21. A power source 22 is connected to the storage capacitance voltage inputting terminal 21. The above-mentioned liquid crystal display matrix panel ordinarily consists of plural signal lines and plural scanning lines wired on a substrate made by such material as glass which cross each other, picture element electrodes provided near each point of

intersection, a first substrate on which the TFTs connected to the signal lines and the scanning lines are wired, a second substrate confronting to the first substrate and having the counter electrodes at the places opposite to the picture element electrodes on the second substrate made by such material as glass and the liquid crystal existing between the picture element electrodes and the counter electrodes. The counter electrodes are other side terminals of the liquid crystals 17 and connected to the auxiliary signal generating circuit 10 .

The operation of the picture element is explained by Fig.2 and Fig.3. When scanning voltage Vg (Vgh, Vgl) turns to the high voltage Vgh, the TFT becomes the ON state and the image signal voltage Vd applied to the signal line 14 is written into the liquid crystal 17. The picture element voltage Vs consequently becomes equal to the image signal voltage Vd. And, when the scanning voltage Vg turns to the low voltage Vgl, the TFT becomes Off state, but the state the Vs scarcely changes(holding state) is kept for a time by the effects of electrostatic capacitance of the liquid crystal and the storage capacitance. As mentioned above, the liquid crystal is driven by the ON or OFF operations of the TFT. The brightness of the liquid crystal is controlled by changing the voltage level of the image signal voltage Vd during the TFT stays at the ON state. The brightness of the liquid crystal 17 depends on the voltage Vlc applied to the liquid crystal, namely, the voltage difference (Vlc=Vs-Vc) between the picture element voltage Vs and the common

voltage Vc applied to the common terminal 19 which is the terminal of the opposite side of the liquid crystal. Therefore, the brightness of the liquid crystal 17 can be controlled by the picture element voltage Vs or the common voltage Vc and full color display is also possible by controlling each voltage Vlc corresponding to each color of R(red), G(green) and B(blue). The constitution of the panel is not restricted to one having such as the two opposite substrates as the embodiment 1.

(Embodiment 2)

Fig.5 shows an embodiment of the present invention of which the equivalent circuit of the picture elements 4 is described as that of Fig.2(b). One picture element is consisted of the TFT 16, the liquid crystal between a picture element 17 electrode and a counter electrode not shown in the figure and the storage capacitance 18, and the total picture elements are arranged in the distributed dots of (m × n) matrix states. A terminal of each liquid crystal 17 is connected to each TFT 16 and the other terminal of the liquid crystal 17 is connected to the auxiliary signal generating circuit 10. A terminal of each storage capacitance 28 is connected to each TFT 16 and the other terminal of the storage capacitance 28 is connected to the scanning line 15 differently from the embodiment 1. Fig.7 shows an example of driving timing for the scanning electrodes and the signal electrodes of the liquid crystal matrix panel, which is common to the embodiments 1 and 2. The scanning voltage Vgl-Vgn are applied in turn to n lines

of the scanning lines 15 for setting the TFTs to ON state so as the voltage Vgh are applied to the TFTs for time TL. The TFTs turn to OFF state for the time(TF-TL) when the scanning voltage is Vgl. The signal voltage Vd(1)-Vd(m) applied to the scanning lines 14 are changed in accordance with the scanning timing and a method for applying the signal voltage is not restricted to any specific one. By the above mentioned driving method, the signal voltage is written to the liquid crystal 17 and the pictures are displayed. Fig.7 shows the fundamental waveform of the voltage Vlc applied to the liquid crystal 17 in the driving apparatus of the present invention. As mentioned above, the voltage Vlc is the difference between the output voltage Vs of TFT 16 and the common voltage Vc and the brightness of the liquid crystal 17 depends on the strength of Vlc, that is, the effective voltage during one period of T2F. The voltage Vlc applied to the liquid crystal 17 consists of the voltage components VN1,VN2 outputted by the first voltage applying means, namely, the signal circuit and the voltage components VB1,VB2 outputted by the second voltage applying means, namely, the auxiliary signal generating circuit 10. The voltages generated by the first voltage applying means drive the liquid crystal for the periods TN1,TN2 and TN3, and the voltages generated by the second applying means drive the liquid crystal for the periods TB1 and TB2. The voltage components VB1,VB2 outputted by the second voltage applying means are applied for the period when all TFTs in the effective picture elements of the

matrix panel are in OFF state. The voltages VN1,VN2 generated by the first voltage applying means shown in Fig.7 change depending on the signal voltage Vd made by video signals. The length of each period of TN1,TN2,TN3 and TN4 when the voltages VN1,VN2 are applied to the liquid crystal is not restricted to any specific value. The waveform of the voltage made by the second voltage applying means is not restricted to any specific shape. That is, the periods TB1,TB2 and the heights of VB1,VB2 are discretional and polarity of the pulse voltages applied to the liquid crystal is not restricted to either mono-polarity or bipolarity. And the driving voltage applying frequency by the second voltage applying means is also discretional. Further the voltages by the first voltage applying means are shown as constant in Fig.7 for the periods TN1,TN2,TN3 and TN4 but the voltages may change with time without detracting the utility of the present invention. The voltage waveform of the picture element by the above-mentioned driving method is explained by using Fig.8. In Fig.8, the equivalent circuit of the picture element and the waveform of each part of the circuit are shown. One picture element consists of the TFT 16, the liquid crystal 17, the storage capacitance 18, the common voltage inputting terminal 19 and the capacitance Cgs 30 between a gate and a source of the TFT. Waveform examples of the voltage driving the circuit and each part of the circuit are shown by the waveforms A,B and C. The waveform A shows the common voltage Vc and one pulse having the amplitude of

±VCN is generated as an auxiliary signal during one frame. The waveforms B show waveforms of the scanning voltage Vg, the image signal voltage Vd and the source voltage Vs. And the waveform C is a waveform of the voltage Vlc which is the difference voltage between the source voltage Vs and the common voltage Vc. As shown in the waveforms B, the source voltage Vs becomes nearly equal to the signal voltage Vd within the period TL when the TFT 16 turns to ON state. After the period, the TFT turns to OFF state and the written voltage is kept. Strictly describing, the source voltage Vs slightly decreases by a resistance of the liquid crystal and a OFF current flowing during the OFF state of the TFT. And the source voltage Vs changes by ±ΔVs as shown in the figure when the common voltage Vc changes by the auxiliary signal Vsub addition in the OFF state of the TFT. The change of ΔVs is described by Eq.(1).

$$\Delta Vs = VCN \cdot (Cs+Clc)/(Cgs+Cs+Clc) \quad .....(1)$$

,where VCN is an amplitude of the auxiliary signal, Cgs is the parasitic capacitance, Cs is the storage capacitance and Clc is the liquid crystal capacitance. And the amplitude of the bias voltage VB is described by Eq.(2)

$$VB = VCN - \Delta Vs \quad .....(2)$$

By applying the bias voltage having the amplitude of VB given by Eq.(2), the effective voltage applied to the liquid crystal is higher than the amplitude Vsig given by the image signal voltage Vd without applying the bias voltage. That is, the higher effective voltage than that voltage inputted only by the outer video signals can be

obtained. The effective value of the applied voltage to the liquid crystal depends on the amplitude and the width of the auxiliary pulse signal Vsub and the effective voltage becomes higher in accordance with increase of the amplitude and the width of a pulse. Fig.9 shows the relation between the image signal voltage amplitude and the effective voltage by comparing two cases with and without the auxiliary signal. Further, Fig.10 shows the relation between the brightness of the liquid crystal and the image signal voltage amplitude. As shown by the curve B in Fig.9, Vos is the effective voltage when Vsig equals 0. Although the effective voltage becomes higher in accordance with increase of the amplitude Vsig, the ratio of the effective voltage deviation to the deviation of the image signal voltage amplitude ($=\Delta Vdr/\Delta Vsig$), namely, the gradient of the curve decreases in accordance with increase of the effective voltage, as compared with the characteristics of the prior driving method, namely, the driving method without the auxiliary signal applying (the curve A). Therefor, as shown by the curve B in Fig.10, the ratio of the liquid crystal brightness change to the change of the image signal voltage amplitude becomes smaller, that is, the characteristics of liquid crystal becomes more gentle, as compared with the characteristics of the prior driving method (the curve A). And the image signal voltage amplitude for getting the same brightness of liquid crystal decreases, as compared with the prior driving method. The brightness and the contrast of a display panel is made

uniform considerably by reducing the brightness variation due to the non-uniformity of the voltage written to liquid crystal caused by the parasitic capacitance between the terminals of TFTs and by the variation of the output voltage of the signal circuit. Thereby it becomes possible to attain the high quality picture display, to downsize the driving circuit, and to lower the power consumption. In Eq.(1), if $(Cs+Clc)/(Cgs+Cs+Clc) \leq 0.5$, then $\Delta Vs \leq VCN/2$,which profitably stabilizes the characteristics of the TFT due to the source voltage fluctuations.

(Embodiment 3)

Fig.11 shows an equivalent circuit of a picture element and driving timing in another embodiment. The embodiment corresponds to Fig.2(b), and one terminal of the storage capacitance is connected to the source terminal S and the other terminal is connected to the scanning line adjoining the scanning line connected to the TFT 16. The auxiliary signal Vsub is applied to the common terminal 19 in the embodiment shown in Fig.5 having the same equivalent circuit shown in Fig.2(b), on the other hand, the auxiliary signal is applied through the scanning line 15 in the present embodiment. The auxiliary signal Vsub of an amplitude VCN smaller than the voltage Vgh besides Vgh,Vgl for turning ON or OFF each TFT is applied to the scanning voltage Vg(i). The voltage Vgh applied as the scanning voltage Vg(i) is transmitted to the source terminal S of the TFT 16 and, synchronizing it, the source voltage Vs is generated. When the source voltage Vg(i+1) becomes Vgh and

the TFT 16 turns to ON state, the image signal is written to the liquid crystal 17 through the signal line 14 and the source voltage Vs becomes the same voltage as the image signal voltage. Nextly, the scanning voltage Vg(i+1) decreases to Vgl and the TFT 16 turns to OFF state, but the written image signal voltage is kept. If the auxiliary signal Vsub is applied to the scanning voltage Vg(i) in the period, the auxiliary signal is transmitted to the source terminal S of the TFT 16 through the storage capacitance 18 and the bias signal is applied to the source voltage, synchronizing to the auxiliary signal Vsub as shown in the figure. The effective voltage applied to the liquid crystal 17 increases and the same effect as the driving method shown in Fig.8 is obtained thereby.

(Embodiment 4)

Fig.12 shows another embodiment in the picture element part. The picture element consists of the scanning line 15, the signal line 14, the TTF 16, the storage capacitance 18 and an auxiliary signal transmitting means 37. The auxiliary signal transmitting means 37 may be composed, for example, by using a condenser Cac for passing alternative current components and cutting off direct current components and the constitution for realizing the means is not restricted to any specific one.

(Embodiment 5)

Fig.13 shows an embodiment as to the auxiliary signal generating circuit 10 and the auxiliary signal information generating means 11 in Fig.4 and Fig.5. In the embodiment,

the auxiliary signal information generating means comprises a variable resistance 32. It is preferable that the variable resistance 32 provided at such places as the outskirts of a display apparatus so as capable of changing the resistance easily. Thereby, it is possible to easily change the brightness, contrast and view angle of the displayed picture.

Embodiments effective for resolving mainly such non-uniform display problems as the smearing in the displayed picture are mentioned in the followings.

(Embodiment 6)

Firstly, the mechanism of the smearing phenomena is briefly explained. The equivalent circuit of the two adjoining picture element in the horizontal direction of the active matrix liquid crystal display apparatus is shown in Fig.28. The picture element electrodes are connected to the source electrodes of the TFTs 16a and 16b, and the picture element electrodes, the counter electrodes and the liquid crystal layers between both the electrodes form the liquid crystal capacitances Clc 17a and 17b. The storage capacitances Cs 18a and 18b are connected to the source electrodes of TFTs 16a and 16b. The counter electrode is common to all picture elements and the earth electrode of the storage capacitance is connected to the (i-1)th scanning line 2 (or the storage line 8). Since the counter electrode potential Vc is common through all picture elements and the earth potentials of the storage capacitances (referred to the storage line potential) Vs

have the same potential, or so at least at the storage line above one line of the line selected presently, the bias voltages of the same polarity are applied to all the picture elements, at least, above one line. And, to the odd number lines and the even number lines, the same polarity of the signal voltages Vd(2j-1) and Vd(2j) are applied, respectively. Thereby, the noise effects become significantly, since the noises to the storage line potentials Vs and the counter electrode potentials Vc induced by changes of the signal voltages Vd(2j-1) and Vd(2j) through the capacitances 100a and 100b between the signal line 3 and the counter electrode and the crossing capacitances 101a and 101b between the signal line 3 and the storage line 28 have the same polarity in the above-mentioned situations. The time that the changing potentials of Vc and Vs revert to the original potential value depends on the change amplitude of the signal voltage Vd and the load conditions of the line above one line. And since each picture element at the line above one line is charged by the same polarity of voltages, the directions of inflow and outflow of the charge current Ion become same and the charge currents Ion flow into the counter electrodes and the storage lines of which potentials are returning to stable state, which prevents the potentials Vs and Vc from reverting to the original value. The voltage written to the picture element is affected by the remaining quantity of the above-mentioned potential variation by the time the TFTs 16a and 16b turn to OFF state, which affects the

variations of the picture element brightness, since the voltage written to the picture elements are determined by the picture element electrode potentials, the counter electrode potentials Vc and the storage line potential Vs at the time the TFTs 16a and 16b turn to OFF state. The variation magnitudes of the signal voltages Vd, the load conditions of the lines and the charge currents which determine the remaining quantity of the above-mentioned potential variation at the time the TFTs turn to OFF state depend on the display picture pattern at the line above one line. Consequently, the poor picture quality such as the striped picture in the horizontal direction, namely, the smearing, which is a sort of cross talk, is brought about. The embodiment shown hereafter considerably reduces the smearing phenomena by dividing the picture elements selected at the same time into two groups and writing the image signal voltages having the polarity reverse to each other into the first group picture element electrodes and the second group picture element electrodes, respectively, because the potential variations(noises) of the counter electrodes and the storage line (or the scanning line), cancel each other or decrease and the charge voltages written into the picture elements are well stabilized due to the short time of potential stabilizing.

Fig.14 shows the circuit constitution of the embodiment and Fig.15 shows an example plane structure of the picture element. As shown in Fig.14, the picture elements between the (i-1)th scanning line and the (i)th

scanning line are divided into two groups, that is, the odd column group and the even column group. The gate electrodes of the TFTs of the odd column group are commonly connected to the (i-1)th scanning line and the earth electrodes of the storage capacitances in the same group are commonly connected to the (i)th scanning line. The gate electrodes of the TFTs of the even column group are commonly connected to the (i)th scanning line and the earth electrodes of the storage capacitances in the same group are commonly connected to the (i-1)th scanning line. The (i) is any integer satisfying the condition: $2 \leq i \leq M$ (M: the whole number of the scanning lines). As far the connective arrangement of the TFTs to the scanning lines, the TFTs of the odd column group are connected to the lower side scanning line and the TFTs of the even column group are connected to the upper side scanning line, that is, the TFTs are connected in zigzag state to a scanning line. The driving LSI 5 for scanning is connected to the scanning lines and the driving LSI 6 of 5 V withstanding voltage for generating the image signal voltages is connected to the signal lines, in the display panel having the above-mentioned constitution. Fig.16 shows waveforms for driving the display panel of the embodiment which are the waveforms of the scanning voltages Vg(i-1),Vg(i) and Vg(i+1) applied to the three adjoining scanning lines, namely, the (i-1)th , the (i)th and the (i+1)th scanning line, and shows the counter electrode potential Vc, the signal voltage Vd(2j-1) applied to the (2j-1)th line,namely, odd column signal line

and the signal Vd(2j) applied to the (2j-1)th line, namely, even column signal line. The scanning signals Vg applied to each scanning line consist of scanning pulses and bipolar bias pulses of the amplitude VB* superposed before and after the scanning pulse(the positive pulse amplitude may be different from the negative pulse amplitude). Therefore, as the driving LSI for scanning, such a LSI as can generate at least four values of voltages is used. Since the liquid crystal must be driven by a alternating current voltage, the voltages having the polarity reverse to each other are applied to the liquid crystals in the odd frame and in the even frame, respectively. As shown in Fig.16, in the odd frame, the waveform superposed by a positive polarity bias pulse of the 1H width before 1H of the scanning pulse of the (1H-td1) width and a negative polarity bias pulse of the (1H+td2) width right after the scanning pulse is applied, and in the even frame, the waveform superposed by a negative polarity bias pulse of the 1H width before 1H of the scanning pulse of the (1H-td1) width and a positive polarity bias pulse of the (1H+td2) width right after the scanning pulse is applied. The rising of the scanning pulse applied to the (i)th scanning line must be done after the scanning pulse applied to the (i-1)th scanning line has dropped sufficiently (the TFT completely turns to OFF state.) and the necessary dropping time is described by td1. And applying the scanning pulse to the (i)th scanning line must be done after the scanning pulse of the same scanning line has dropped sufficiently and the necessary

dropping time is described by td2. For example, 3 μs is adopted as the value of td1 and td2. Further, the signal voltage Vd must be changed after the scanning pulse applied to the former scanning line has dropped sufficiently, when signals are written into picture elements selected by the next scanning line after writing image signals into picture elements selected by a scanning line is finished. The necessary dropping time is assumed as the same time as td2. The amplitude VB^* of the bias pulse is set up as follows so as the maximum amplitude Vdpp (Vdpp=Vmax-Vth) of the voltage applied to the scanning line becomes minimum, corresponding to the characteristics curve of transmitted light strength-voltage applied to liquid crystal shown in Fig.27. The voltage actually applied to the liquid crystal is given by the following equation from the bias voltage VB^* applied to the scanning line.

$$VB=(Vmax+Vth)/2 \quad .....(3)$$

where Vth is the optical threshold voltage in the characteristics curve of transmitted light strength-voltage applied to liquid crystal shown in Fig.27 and Vmax is the voltage for obtaining black color display in normally opened state. Since the counter electrode potential Vc is constant in the embodiment, VB^* for obtaining the bias voltage VB is described by the following equation.

$$VB^*=VB\cdot(Cs+Clc+Cgs)/Cs....(4)$$

where Cgs is the gate-source capacitance of the TFT. For example, if the liquid crystal of which Vth is 2 V is used and Vmax is set, then Vdpp=3 V and VB=3.5 V are

obtained. Therefor, if the picture element where Cs=3 Clc is designed, the amplitude VB^* of the bias voltage is obtained since Cgs<<Cs,Clc. In this case, Vdpp< 5 V, so cheap LSIs of 5 V withstanding voltage can be used and, further more, the contrast ratio 60 can be obtained. In the waveforms in Fig.16, in the odd frame, when the scanning pulse is applied to the (i)th scanning line, the positive bias voltage VB^* is applied to the (i+1)th line and the negative bias voltage ($-VB^*$) is applied to the (i-1)th scanning line. And the voltages of the polarity reverse to each other $\pm Vsig^*$ ($=\pm VB^*\pm Vd$: double sign is in the same order.) are written into the storage capacitances of the odd column picture elements and the even column picture elements, respectively, by applying the positive signal voltage (+Vd) to the even column signal lines and the negative signal voltage (-Vd) to the odd column signal lines. In the picture elements selected at the same time, the positive bias voltage and the negative signal voltage are applied to the odd column picture element, and the negative bias voltage and the positive signal voltage are applied to the even column picture elements. Each polarity of the bias voltage and the signal voltage is reverse to each other. And when the potentials of the (i-1)th, the (i)th, and the (i+1)th scanning line turn to OFF level, the image signal voltages of the polarity reverse to each other $\pm Vsig$($=\pm VB\pm Vd$: double sign is in the same order.) are applied to the odd column picture elements and the even column picture elements, respectively and the light

transmission rate is controlled thereby. The voltage Vd expresses the potential deviation from the central voltage Vd-center, its value is 1.5 V in black color displaying and -1.5 V in white color displaying. The polarity of the bias voltages and the signal voltages in the odd frame turn over in the even frame. Since, in the embodiment, the constitution having the TFTs arranged in zigzag state at a scanning line, the sequence means fitted to such TFT arrangement for addressing the image signal data is provided in the image signal generating part. As mentioned above, the good contrast ratio can be obtained while the voltage amplitudes applied to the signal lines are decreased. Further, by turning over the polarity of the signal voltages written into the picture elements every column in a frame, the noises induced within the period 1H at the potentials of the counter electrodes and the scanning line through the capacitances between the signal electrodes and the scanning line induced by change of the signal voltage Vd cancel each other between the adjoining picture elements in the horizontal direction . The noises induced within the period 1H at the counter electrodes by the current flowing into the counter electrodes through the liquid crystal capacitances due to the one way nature of the charge current in the image signal writing also cancel each other between the adjoining picture elements. And, as far the effects of the noises induced within the period 1H at the potential of the scanning line by the current flowing into the scanning line through the storage

capacitances due to the one way nature of the charge current in the image signal writing, the ability of absorbing noises increases by about two times and the potential stabilizing time become shorter since the noise effects decrease more rapidly, by the constitution of the embodiment. Thereby, the dependency of the voltages written into the picture elements on the display signal pattern in the horizontal direction is reduced and consequently, the smearing generated in the horizontal direction is considerably decreased. In the embodiment, a-Si TFTs are used as transistor elements but the transistor elements is not restricted to any specific type. For example, p-Si TFT or MOS FET may be used. Although the picture elements are divided into the odd column group (the first group) and the even column group (the second group) in the embodiment, the dividing way is not restricted to any specific way and only two group dividing is necessary. For example, by bundling the consecutive n columns (n=1,2,3,...)in one unit, dividing the units into the odd number unit group and the even number unit group is a usable way. In the way, the bias voltages of the polarity reverse to each other through the storage capacitances and the signal voltages of the polarity reverse to each other are also applied to the picture elements of the first group and the second group, respectively. And the bias voltage and the signal voltage applied to the same picture element have the polarity reverse to each other. Such a grouping way as the number of the picture elements in each group is equal makes the noise

canceling effect great and the grouping way that n=1 makes the effect maximum.

(Embodiment 7)

The constitution of the embodiment is the same as the embodiment 6 except the matters mentioned in the following.

The embodiment 6 has the constitution having the TFTs arranged in zigzag state at a scanning line and the sequence means fitted to such TFT arrangement for addressing the image signal data is provided in the image signal generating part. But, for making the display apparatus compatible with the signal generating part of a usual personal computer, it is necessary to delay the odd column image signal data after the even column image signal data by the period 1H in the above-mentioned constitution of the embodiment 6. In the present embodiment, as shown in Fig.17, the even column image signal data outputted from the controller 8 are held on the bus line for inputting the data to the lower signal driving LSI 6 during the period 1H by using the 1/2 line memories 62 and inputted to the lower signal driving LSI 6. And the non-interlaced signals are used as the image signal data. Although the 1/2 line memories are used in the embodiment, the memories 62 may be provided in the controller 8. The embodiment has the effects that the display apparatus of the embodiment can be connected to a general purpose image signal generating part of such a computer as a personal computer in addition to the effects of the embodiment 6.

(Embodiment 8)

The constitution of the embodiment is the same as the embodiment 6 except the matters mentioned in the following.

For matching the matrix constitution having the TFTs arranged in zigzag state at a scanning line, a signal driving LSI 6 is used. The signal driving LSI 6 has a shift resistor or a latch 71 for memorizing the image signals in turn, a latch 73 for memorizing the image signals Vd fitting to the horizontal synchronizing signal, latch 72 capable of selecting a latching or a passing through mode and a sample hold circuit or a voltage selector for generating the image signal 74. By setting the latch 72 to the passing through mode in the upper signal driving LSI and to the latching mode in the lower driving LSI, the image signals Vd from the lower driving LSI is delayed by the period 1H. The present embodiment as well as the embodiment 7 has the effects that the display apparatus of the embodiment can be connected to a general purpose image signal generating part of such a computer as a personal computer in addition to the effects of the embodiment 6.

(Embodiment 9)

The constitution of the embodiment is the same as the embodiment 6 except the matters mentioned in the following.

In Fig.19, the driving waveforms are shown in the embodiment. The scanning lines are scanned at every two lines (interlaced). Thereby, it is not necessary to wait the sufficient dropping of the previous scanning pulse for generating the next scanning pulse and the waiting period

td1 shown in Fig.16 is not necessary. And the capacitances of the liquid crystals and the storage capacitances is charged enough, which prevents the poor charging, since the scanning pulse width can be increased by the period td1 (for example, 3 μs) by the above-mentioned scanning. The image signals of 1/2 frame in the even column signal lines are memorized and outputted to each even column signal line by memorizing the interlaced signals using the 1/4 frame memories in the embodiment. The present embodiment, in addition to the effects of the embodiment 6, has the effects that the display apparatus decreases the poor charging and suppresses the brightness uniformity.

(Embodiment 10)

The constitution of the embodiment is the same as the embodiment 6 except the matters mentioned in the following.

In the embodiment, the polarity of the signal voltages is turned over at every column and the polarity of the bias pulses is also turned over at every column. The generated waveforms are shown in Fig.20. By turning over the polarity of the image signal voltages at every column, the noises induced by the signal voltages Vd in one frame at the picture element voltages through the capacitances between the picture element electrodes and the signal lines are averaged over the frame and the vertical smearing depending on the display image pattern in the column direction besides the horizontal smearing can be also suppressed. The present embodiment, in addition to the effects of the embodiment 6, has the effects that the display apparatus

suppresses also the vertical smearing.

(Embodiment 11)

The constitution of the embodiment is the same as the embodiment 6 except the matters mentioned in the following.

The plane constitution of the picture elements in the embodiment is shown in Fig.21. The picture element electrode 50 which has two aperture parts is formed at the both sides of a TFT in the column direction by crossing the TFT. Thereby, the picture elements scanned at the same scanning line are partially overlapped by each other and, at the same time, the storage capacitances Cs at the odd column and the storage capacitances Cs at the even column are connected to the different scanning lines, respectively. The present embodiment has the same constitution of electrical circuit as the embodiment 6 but the spatial constitution different from that of the embodiment 6. The present embodiment can display the display image pattern correctly without shifting each phase of the signal voltages of the odd column and the even column by the period 1H, by remedying spatially the effects by the time lag of the period 1H between the signal voltages of the odd column and the even column. The present embodiment, in addition to the effects of the embodiment 6, has the effects that the display apparatus can present the lower cost module comprising the controllers and so forth since the phase shifting of the signal voltages of the odd column and the even column by the period 1H is not needed and the 1/2 line memories or the 1/4 frame memories have

not to be provided as in the embodiments 7 and 9.

(Embodiment 12)

The circuit diagram of the active matrix liquid crystal display apparatus of the embodiment is shown in Fig.22. By forming the counter electrodes in stripe state and grouping them into the odd column electrodes and the even column electrodes, each group is commonly connected to the first bias circuit 53 and the second bias circuit 54, respectively. And the storage capacitances Cs are formed by the gate insulating film sandwiched between the wiring (storage wiring) constituted by the same material and layer as the scanning wiring and the picture elements, and the odd column storage capacitances are commonly connected to the storage lines S1 and the even column storage capacitances are commonly connected to the storage lines S2. All the storage lines S1 are connected together and to the first bias circuit 53, and all the storage lines S2 are connected together and to the second bias circuit 54. Although the picture elements at the same line are divided into the odd column group (the first group) and the even column group (the second group) in the embodiment, the dividing way is not restricted to any specific way and only two group dividing of the picture elements selected at the same time and on the same scanning line is necessary. Particularly, if the column picture elements are divided two groups in every column as described in the embodiment, the flickering is most effectively suppressed due to short turning over period of the polarity. However, the column

grouping in every column brings about the high probability of short-circuits, so it is preferable to determine the number of burdening the columns by considering the trade-off between the flickering suppressing and the short circuit decreasing. In Fig.23, the driving waveforms are shown. The rectangular waveform voltages Vs and Vc having the amplitude 2 VB^* outputted from the first and the second bias circuit are applied to the storage lines and the counter electrodes by the alternating period at two frames. The phase shift between the voltage waveforms outputted from the first bias circuit 53 and the second bias circuit 54 is 180 degrees (each polarity of the voltages is reverse to each other.) and the voltages of the polarity reverse to each other are superposed to the signal voltages of the odd column and the even column picture elements, respectively. Since the liquid crystal needs to be driven by an alternating current voltage, the voltages of the polarity reverse to each other are superposed to the liquid crystals in the odd frame and in the even frame, respectively. The polarity turning over is done during the period of retrace line. And the signal voltages outputted to the odd column and the even column signal lines have the polarity reverse to each other and are turned over in every frame. The bias pulse amplitude 2 VB^* is set according to the characteristics curve of transmitted light strength-applied voltage so as the bias voltage VB is within the range $Vth \leq VB \leq Vmax$ and the maximum amplitude Vdpp of the voltages applied to the signal lines is the minimum value

(Vdpp=Vmax-Vth). First, the amplitude 2 VB is determined by Eq.(3) similarly in the embodiment 6. Let Cgs<<Cs,Clc (Cgs: capacitance between TFTs, Cs: storage capacitance, Clc: liquid crystal capacitance), and the bias voltage VB(=VB*) is given by the bias pulse amplitude 2 VB* as the voltage applied to the liquid crystal. For example, by using the liquid crystal of which Vth is 2 V and setting Vmax=5 V, Vdpp=3 V and VB=3.5 V are obtained. And the bias pulse amplitude 2 VB* is set to 7 V. For turning over the polarity of the odd column signal voltage and the polarity of the even column signal voltage in every column, respectively, it is adoptable that, by dividing the signal driving LSI into the upper one and the lower one and connecting the odd column signal lines to the upper signal driving LSI, and the even column signal lines to the lower signal driving LSI, the voltages outputted from the upper signal driving LSI and the lower signal driving LSI have the polarity reverse to each other. By controlling the polarity of the image signal voltages so as the voltages ±Vsig(=VB±Vd, double sign is in the same order.) are applied as the image signal voltage, the polarity of the image signal voltages is turned over in every column, where Vd is the potential difference from the center voltage Vd-center, its value is 1.5 V in black color displaying and -1.5 V in white color displaying. And, by the embodiment, the contrast ratio of 60 is gained and, further, the LSIs of 5 V withstanding voltage can be used since Vdpp= 3 V and the cost spent for LSIs can be also reduced.

(Embodiment 13)

The circuit diagram of the active matrix liquid crystal display apparatus of the embodiment is shown in Fig. 24. The counter electrode is formed all over the picture elements. The storage capacitances Cs are formed by the storage lines, the picture element electrodes and the gate insulating film between them, and the odd column picture elements are connected to the storage lines S1 and the even column picture elements to the storage lines S2. The storage lines S1 and S2 are respectively connected to the bias signal driving LSI 40 in every column thereof insulated electrically. Fig.25 shows the driving waveforms of the embodiment. The bias pulses from the bias signal driving LSI 40 are applied to each storage lines when the line is selected. So as the voltage of the polarity reverse to each other are superposed to the picture elements of the odd column and the even column, respectively, the polarity of the bias pulses applied to the storage lines S2 is made reverse to the polarity of the bias pulses of the storage lines S2. And the bias voltages of the polarity reverse to each other are applied to the liquid crystals in the odd frame and in the even frame, respectively , since the liquid crystal needs to be driven by an alternating current voltage. Since the counter electrode is common to all the picture elements in the embodiment, the counter electrode potential is set constant and the two voltages of the different polarity are supplied as the bias voltage only through the storage capacitances. The bias pulse amplitudes

$VB^*(+)$ and $VB^*(-)$ are set as follows. First, the bias voltages applied to the liquid crystals are set by Eq.(3) similarly in the embodiment 6. And, let $VB^*(+) + VB^*(-)=2VB^*$, particularly $VB(+)^*=VB^*(-)=VB^*$, the relation between VB^* and VB is given by Eq.(4). For example, by using the liquid crystal of which Vth is 2 V, VB=3.5 V is obtained. And, by using the picture element of which Cs equals 3 Clc, VB^* is set 4.7 V for setting VB 3.5 V since Cgs<<Cs,Clc. By controlling the polarity of the image signal voltages so as the voltages ±Vsig (=VB±Vd, double sign is in the same order.) are applied as the image signal voltage, the polarity of the image signal voltages is also turned over in every column in the present embodiment similarly in the embodiment 12. And the bias pulses must be dropped after the TFTs of the lines to which the pulses are applied completely turn to OFF state. The maximum delay time td is, for example, 3 μs and the bias pulse width is set (1H+td). And, by the embodiment, the contrast ratio of 60 is gained and, further, the LSIs of 5 V withstanding voltage can be used since Vdpp < 5 V. Further, by the constitution of the present embodiment, the product process for dividing the counter electrodes is not needed, so the panel product cost can be reduced by throughput improvement, decrease of material cost such as resist material and yield rate improvement.

(Embodiment 14)

The constitution of the embodiment is the same as the embodiment 13 except the matters mentioned in the

following. Fig.26 shows the plane pattern of the storage capacitance part in the embodiment. The storage capacitance consists of the scanning line or the storage line in the same layer as the scanning line, a part of the picture element and the gate insulating film. Since the scanning line the picture element electrode lie in the different layers, the storage capacitance depends on places of the panel due to the inaccuracy of photo-mask alignment, which changes the bias voltage. The bias voltage variation induces the brightness non-uniformity in block state. By the embodiment, as shown in Fig.26, such a plane pattern is presented as the intersecting area of the picture element electrode and the storage line in the same layer as the scanning line does not change even if the photo-mask shifts before and behind, and left and right.

The present embodiment, in addition to the effects of the embodiment 6, has the effects that the display apparatus can present the picture without the block non-uniformity.